AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (previously presented) A method of routing a system bus to a plurality of expansion cards, said method comprises the acts of:

routing the bus into a first connector and into a first circuit card residing within the first connector;

routing the bus from a portion of the first circuit card into a portion of a second circuit card residing within a second connector, wherein the bus is routed from the first circuit card to the second circuit card without entering the second connector; and

routing the bus through the second circuit card to the second connector.

2. (original) The method of claim 1 further comprising the acts of:

routing the bus into a third connector and into a third circuit card residing within the third connector;

routing the bus from a portion of the third circuit card into a portion of a fourth circuit card residing within a fourth connector, wherein the bus is routed from the third circuit card to the fourth circuit card without entering the fourth connector;

routing the bus through the fourth circuit card to the fourth connector; and

routing the bus out of the fourth connector.

3. (original) The method of claim 1 further comprising the acts of:

routing the bus into a third connector and into a third circuit card residing within the third connector; and

routing the bus from a portion of the third circuit card into a portion of a system circuit board.

4. (original) The method of claim 1 further comprising the act of routing the bus out of the second connector into a portion of a system circuit board.

5. (original) The method of claim 4 further comprising the act of terminating the bus after routing the bus out of the second connector.

6. (original) The method of claim 1 wherein the first and second circuit cards each contain a top edge portion, each top edge portions being opposite an edge portion residing in a respective connector, and wherein the bus is routed from the top edge portion of the first circuit card into the top edge portion of the second circuit card.

7. (original) The method of claim 1 wherein the first and second circuit cards each contain a top edge portion, each top edge portions being opposite a bottom edge portion residing in a respective connector, and wherein the bus is routed from a portion between the top and bottom edges of the first circuit card into a portion between the top and bottom edges of the second circuit card.

8. (original) The method of claim 1 wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a jumper mechanism.

9. (original) The method of claim 1 wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a circuit board having bus portion traces for continuing the bus between the first and second circuit cards.

10. (original) The method of claim 1 wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a cable.

11. (original) The method of claim 1 wherein at least address, data and control signals are routed on said bus between the first and second circuit cards.

12. (original) The method of claim 11 wherein only address, data and control signals are routed on said bus between the first and second circuit cards.

13. (original) The method of claim 1 wherein address, data, control and power signals are routed on said bus between the first and second circuit cards.

14. (previously presented) A method of routing a system bus to a plurality of expansion cards provided on a motherboard of the system, said method comprises the acts of:

routing the bus into a first circuit card residing within a first slot;

routing the bus from a portion of the first circuit card into a portion of a second circuit card residing within a second slot, wherein the bus is routed from the first circuit card to the second circuit card without entering the second slot; and

routing the bus through the second circuit card.

15. (original) The method of claim 14 further comprising the acts of:

routing the bus into a third circuit card residing within a third slot;

routing the bus from a portion of the third circuit card into a portion of a fourth circuit card residing within a fourth slot, wherein the bus is routed from the third circuit card to the fourth circuit card without entering the fourth slot; and

routing the bus through and out of the fourth circuit card.

16. (original) The method of claim 14 further comprising the acts of:

routing the bus into a third circuit card residing within a third slot; and

routing the bus from a portion of the third circuit card into a portion of the motherboard.

17. (original) The method of claim 14 further comprising the act of routing the bus out of the second slot.

18. (original) The method of claim 17 further comprising the act of terminating the bus after routing the bus near either or both ends of the bus.

19. (original) The method of claim 14 wherein the first and second circuit cards each contain a top edge portion, each top edge portions being opposite an edge portion residing in a respective slot, and wherein the bus is routed from the top edge portion of the first circuit card into the top edge portion of the second circuit card.

20. (original) The method of claim 14 wherein the first and second circuit cards each contain a top edge portion, each top edge portions being opposite a bottom edge portion residing in a respective slot, and wherein the bus is routed from a portion between the top and bottom edges of the first circuit card into a portion between the top and bottom edges of the second circuit card.

21. (original) The method of claim 14 wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a jumper mechanism.

22. (original) The method of claim 14 wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a circuit board having bus portion traces for continuing the bus between the first and second circuit cards.

23. (original) The method of claim 14 wherein said act of routing the bus from the portion of the first circuit card into the portion of the second circuit card comprises connecting the portion of the first circuit card to the portion of the second circuit card by a cable.

24. (original) The method of claim 14 wherein at least address, data and control signals are routed between the first and second circuit cards.

25. (original) The method of claim 24 wherein only address, data and control signals are routed on said bus between the first and second circuit cards.

26. (original) The method of claim 14 wherein address, data, control and power signals are routed on said bus between the first and second circuit cards.

27. (original) The method of claim 14 wherein the bus is routed into the first circuit card by routing the bus into a first connector in which the first circuit card is residing.

28. (original) The method of claim 14 wherein the bus is routed out of the second circuit card by routing the bus out into a second connector in which the second circuit card is residing.

29. (original) The method of claim 14 wherein a first portion of bus signals are routed between the first and second circuit cards and a second portion of bus signals are provided to the second circuit card from the motherboard.

Claims 30-35 (canceled).

36. (original) A bus system comprising:

a bus mounted on a circuit board of said system; and

a plurality of expansion slots, each slot comprising a connector mounted on said circuit board and a circuit card residing within the connector, wherein said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector and through said second circuit card, and wherein said bus is routed from said first circuit card to said second circuit card without entering said second connector.

37. (original) The system of claim 36 further comprising:

a third connector having a third circuit card residing therein; and

a fourth connector having a fourth circuit card residing therein, wherein said bus is further routed into said third connector to said third circuit card, out of a portion of said third circuit card into a portion of said fourth circuit, through said fourth circuit card and out of said fourth connector, and wherein said bus is routed from said third circuit card to said fourth circuit card without entering said fourth connector.

38. (original) The system of claim 36 further comprising a third connector having a third circuit card residing therein, wherein said bus is further routed into said third connector to said third circuit card, out of a portion of said third circuit card and into a portion of said system circuit board.

39. (original) The system of claim 36 wherein said bus is terminated by a plurality of resistors.

40. (original) The system of claim 36 further comprising a jumper mechanism connected between said portions of said first and second circuit cards, said jumper mechanism for routing said bus between said first and second circuit cards.

41. (original) The system of claim 40 wherein said portions are located at a top edge of said first and second circuit cards opposite a bottom edge residing in said connectors.

42. (original) The system of claim 40 wherein said first and second circuit cards each contain a top edge portion, each top edge portions being opposite a bottom edge portion residing in a respective connector, and wherein said bus is routed from a portion between said top and bottom edges of said first circuit card into a portion between said top and bottom edges of said second circuit card.

43. (original) The system of claim 40 wherein said jumper mechanism comprises:

a circuit board having bus portion traces configured for continuing said bus between said first and second circuit cards; and

a plurality of connectors coupled to said circuit board, at least one connector adapted to receive said portion of said first circuit card and at least one other connector adapted to receive said portion of said second circuit card.

44. (original) The system of claim 40 wherein said jumper mechanism comprises:

a cable configured for continuing said bus between said first and second circuit cards; and

a plurality of connectors coupled to said cable, at least one connector adapted to receive said portion of said first circuit card and at least one other connector adapted to receive said portion of said second circuit card.

45. (original) The system of claim 44 wherein said cable is a ribbon cable.

46. (original) The system of claim 44 wherein said cable is a ribbon cable with a shield.

47. (original) The system of claim 44 wherein said cable is a coaxial cable.

48. (original) The system of claim 44 wherein said cable is a twisted pair wiring.

49. (original) The system of claim 44 wherein said cable is a waveguide.

50. (original) The system of claim 36 wherein said circuit cards are dynamic random access memory circuit cards and said system further comprises a memory controller coupled to said bus.

51. (original) A bus system comprising:

a bus mounted on a circuit board of said system; and

a plurality of expansion slots mounted on said circuit board, wherein said bus is routed into a first circuit card residing within a first slot, out of a portion of said first circuit card and into a portion of a second circuit card residing within a second slot

and out of the second circuit card, wherein said bus is routed from said first circuit card to said second circuit card without entering said second slot.

52. (original) The system of claim 51 further comprising:

a third slot having a third circuit card residing therein; and

a fourth slot having a fourth circuit card residing therein, wherein said bus is further routed into said third circuit card, out of a portion of said third circuit card and into a portion of said fourth circuit, and out of said fourth circuit card, wherein said bus is routed from said third circuit card to said fourth circuit card without entering said fourth slot.

53. (original) The system of claim 51 further comprising a third slot having a third circuit card residing therein, wherein said bus is further routed into said third circuit card, out of a portion of said third circuit card and into a portion of said system circuit board.

54. (original) The system of claim 51 wherein said bus is terminated by a plurality of resistors.

55. (original) The system of claim 51 further comprising a jumper mechanism connected between said portions of said first and second circuit cards, said jumper mechanism for routing said bus between said first and second circuit cards.

56. (original) The system of claim 55 wherein said portions are located at a top edge of said first and second circuit cards, said top edges being opposite respective bottom edges residing in associated slots.

57. (original) The system of claim 55 wherein said portions are located between top and bottom edges of said cards, said top edges are opposite respective ones of said bottom edges, said bottom edges residing with a respect slot.

58. (original) The system of claim 55 wherein said jumper mechanism comprises:

a circuit board having bus portion traces configured for continuing said bus between said first and second circuit cards; and

a plurality of connectors coupled to said circuit board, at least one connector adapted to receive said portion of said first circuit card and at least one other connector adapted to receive said portion of said second circuit card.

59. (original) The system of claim 55 wherein said jumper mechanism comprises:

a cable configured for continuing said bus between said first and second circuit cards; and

a plurality of connectors coupled to said cable, at least one connector adapted to receive said portion of said first circuit card and at least one other connector adapted to receive said portion of said second circuit card.

60. (original) The system of claim 59 wherein said cable is a ribbon cable.

61. (original) The system of claim 59 wherein said cable is a ribbon cable with a shield.

62. (original) The system of claim 59 wherein said cable is a coaxial cable.

63. (original) The system of claim 59 wherein said cable is a twisted pair wiring.

64. (original) The system of claim 59 wherein said cable is a waveguide.

65. (original) The system of claim 51 wherein said circuit cards are dynamic random access memory circuit cards and said system further comprises a memory controller coupled to said bus.

66. (original) A processor-based system comprising:

a processor; and

a bus system coupled to said processor; said bus system comprising:

a bus mounted on a circuit board of said system; and

a plurality of expansion slots, each slot comprising a connector mounted on said circuit board and a circuit card residing within the connector, wherein said bus is routed into a first connector, into a first circuit card residing within said first connector, out of a portion of said first circuit card into a portion of a second circuit card residing within a second connector, through said second circuit card and out of said second connector, wherein said bus is routed from said first circuit card into said second circuit card without entering said second connector.

67. (original) A processor-based system comprising:

a processor; and

a bus system coupled to said processor; said bus system comprising:

a bus mounted on a circuit board of said system; and

a plurality of expansion slots mounted on said circuit board, wherein said bus is routed into a first circuit card residing within a first slot, out of a portion of said first circuit card and into a portion of a second circuit card residing within a second slot

and out of the second circuit card, wherein said bus is routed from said first circuit card into said second circuit card without entering said second slot.

68. (original) A processor-based system comprising:

a processor; and

a memory bus system coupled to said processor; said bus system comprising:

a bus mounted on a circuit board of said system; and

a plurality of expansion slots mounted on said circuit board, wherein said bus is routed into a first memory circuit card residing within a first slot, out of a portion of said first memory circuit card and into a portion of a second memory circuit card residing within a second slot, and out of the second memory circuit card, wherein said bus is routed from said first memory circuit card into said second memory circuit card without entering said second slot.

Claims 69-72 (canceled).